WHAT IS CLAIMED IS:

1. A computing device, comprising:
   a) a set of at least two masters;
   b) at least one target;
   c) at least one bus providing connection between the masters and the target;
   d) a system controller operable to quiesce masters from the set of masters in response to an error message; and
   e) a system error processor operable to handle an error condition indicated by the error message.
2. The device of claim 1, wherein the set of masters includes at least one direct memory access controller.
3. The device of claim 1, wherein the set of masters includes at least one peripheral component interconnect controller.
4. The device of claim 1, wherein at least one bus includes a peripheral component interconnect bus.
5. The device of claim 1, wherein the error message causing the system controller to quiesce the selected masters is programmable.
6. A computing device, comprising:
   a) at least one means for receiving and providing data;
   b) a set of means for addressing the means for receiving and providing data;
   c) a means for providing connection between the set of means for receiving and providing data and the at least one means for addressing;
   d) a means for quiescing masters from the set of masters in response to an error message; and
   e) a means for handling an error condition indicated by the error message.

7. The device of claim 6, wherein the error message causing the system controller to quiesce the selected masters may be programmable.

8. A method for automatically quiescing selected masters in a multimaster device, the method comprising:

a) receiving an error message indicating an error condition has arisen;

b) determining if the error message is one which triggers auto quiesce; and

c) generating auto quiesce signals to stop operations in the selected masters.

9. The method of claim 8, wherein the method further comprises re-enabling the selected masters after the error condition has been cleared.

10. The method of claim 8, wherein the error message is an interrupt.

11. The method of claim 8, wherein determining if the error message further is one which triggers auto quiesce further comprises preconfiguring a system controller with the error messages.

12. The method of claim 8, wherein generating auto quiesce signals further comprises signaling an address arbiter to halt address grants for the selected masters.